PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
KEN W. MARR

Serial No.: Unknown

Filed: Concurrently Herewith

For: ADJUSTABLE HIGH-TRIGGER-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION DEVICE

Group Art Unit: Unknown

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PRELIMINARY AMENDMENT

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I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage"EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington D.C. 20231.

Mary Paul
Signature

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-captioned application as follows:

IN THE CLAIMS:

Please amend claim 35 as follows:

35. (Amended) A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

forming a first doped plug in the first doped region;

forming a second doped plug in the first doped region; and

forming an isolation structure between the first and second doped plugs.

Please add new claims 44-54 as follows:

44. (New) A method comprising:

providing a p-type semiconductor substrate;

forming a first n-well within the p-type semiconductor substrate;

forming a first n-plug within the first n-well;

forming a second n-plug within the p-type semiconductor substrate; and

forming an isolation structure between the first and second n-plugs.

45. (New) The method of claim 44, further comprising forming a second n-well within the p-type semiconductor substrate, wherein forming the second n-plug within the p-type semiconductor substrate comprises forming a second n-plug within the second n-well.

46. (New) The method of claim 44, wherein forming the first n-plug within the first n-well comprises forming the first n-plug a first distance from a first boundary of the first n-well, wherein a breakover voltage between the first n-plug and the p-type semiconductor substrate depends on the first distance.

47. (New) The method of claim 44, wherein forming the isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

48. (New) The method of claim 44, wherein forming an isolation structure comprises forming a gate terminal.

49. (New) The method of claim 48, wherein forming a gate terminal comprises:

forming a dielectric layer adjacent at least a portion of the semiconductor substrate; and

forming a conductor layer above at least a portion of the dielectric layer.

50. (New) The method of claim 44, further comprising forming a conductor layer above at least a portion of the first and second n-plugs.

51. (New) A method for forming an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first doped region in the semiconductor substrate;

forming a first doped well within the first doped region;

forming a first doped plug at a selected location within the first doped well, wherein the selected location is selected to provide a first breakover voltage between the first doped plug and the first doped region;

forming a second doped plug within the first doped region;

forming an isolation structure between the first and second doped plugs;

forming a bond pad on the semiconductor substrate;

forming a voltage source node on the semiconductor substrate;

coupling the first doped plug to the bond pad;

coupling the second doped plug to the voltage source node; and

forming at least one integrated circuit component on said semiconductor substrate coupled to the bond pad.

52. (New) The method of claim 51, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug within the first doped region comprises forming the second doped plug within the second doped well.

53. (New) The method of claim 51, wherein forming an isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

54. (New) The method of clam 51, wherein forming at least one integrated circuit component comprises forming an anti-fuse network.

REMARKS

The fees believed to be due in connection with the filing of this Preliminary Amendment are included in the amount calculated in the Request for Filing Divisional Application. However, should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Assistant Commissioner is hereby authorized to deduct said fees from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2008.000282.

The Examiner is invited to contact the undersigned attorney at (713) 934-4060 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: August 20, 2001

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AMENDED AND NEW CLAIMS

35. (Amended) A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

forming a first doped plug in[to] the first doped region;

forming a second doped plug in[to] the first doped region; and

forming an isolation structure between the first and second doped plugs.

44. (New) A method comprising:

providing a p-type semiconductor substrate;

forming a first n-well within the p-type semiconductor substrate;

forming a first n-plug within the first n-well;

forming a second n-plug within the p-type semiconductor substrate; and

forming an isolation structure between the first and second n-plugs.

45. (New) The method of claim 44, further comprising forming a second n-well within the p-type semiconductor substrate, wherein forming the second n-plug within the p-type semiconductor substrate comprises forming a second n-plug within the second n-well.

46. (New) The method of claim 44, wherein forming the first n-plug within the first n-well comprises forming the first n-plug a first distance from a first boundary of the first n-well, wherein a breakover voltage between the first n-plug and the p-type semiconductor substrate depends on the first distance.

47. (New) The method of claim 44, wherein forming the isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

48. (New) The method of claim 44, wherein forming an isolation structure comprises forming a gate terminal.

49. (New) The method of claim 48, wherein forming a gate terminal comprises:

forming a dielectric layer adjacent at least a portion of the semiconductor substrate; and

forming a conductor layer above at least a portion of the dielectric layer.

50. (New) The method of claim 44, further comprising forming a conductor layer above at least a portion of the first and second n-plugs.

51. (New) A method for forming an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first doped region in the semiconductor substrate;

forming a first doped well within the first doped region;

forming a first doped plug at a selected location within the first doped well, wherein the selected location is selected to provide a first breakover voltage between the first doped plug and the first doped region;

forming a second doped plug within the first doped region;

forming an isolation structure between the first and second doped plugs;

forming a bond pad on the semiconductor substrate;

forming a voltage source node on the semiconductor substrate;

coupling the first doped plug to the bond pad;

coupling the second doped plug to the voltage source node; and

forming at least one integrated circuit component on said semiconductor substrate coupled to the bond pad.

52. (New) The method of claim 51, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug within the first doped region comprises forming the second doped plug within the second doped well.

53. (New) The method of claim 51, wherein forming an isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

54. (New) The method of clam 51, wherein forming at least one integrated circuit component comprises forming an anti-fuse network.